

V N S S S R Maheedhar Bhamidipati

M.Tech VLSI Design (2025) | Amrita Vishwa Vidyapeetham

+91-7416964632 | maheedharbh@gmail.com | linkedin.com/in/maheedhar-bhamidipati |
github.com/MaheedharBhamidipati | https://maheedhar-bhamidipati-portfolio.netlify.app/

SUMMARY

M.Tech VLSI Design graduate (2025) with pre-silicon DV and RTL design experience; developed UVM/SystemVerilog testbenches achieving **96% functional coverage** and isolated **4 pre-synthesis RTL bugs** across CNN, k-NN, and Decision Tree inference accelerator modules. Skilled in SVA, constrained-random verification, AXI4 protocol, and RTL synthesis with Cadence Genus; validated designs on Xilinx ZYNQ-7000 FPGA.

TECHNICAL SKILLS

Verification: SystemVerilog, UVM, SVA, Constrained-Random Verification, Functional & Code Coverage, Coverage-Driven Verification (CDV), Regression Testing, Testplan Development, Gate-Level Simulation (GLS), Formal Verification (Basics), Pre-Silicon Validation

RTL Design: Verilog, FSM Design, RTL Micro-Architecture, RTL Synthesis, Static Timing Analysis (STA), PPA Analysis, Low-Power Design (Clock Gating, Operand Isolation), Physical Design Flow (RTL-to-GDS)

EDA Tools: ModelSim, QuestaSim, Xilinx Vivado, Cadence Genus, Cadence Virtuoso, Linux (CLI, scripting)

Protocols: AXI4, APB, SPI, I2C, UART, RS-485, AMBA Bus Architecture

Scripting: Python (verification automation, golden modeling, coverage analysis), TCL (EDA scripting)

Hardware: Xilinx ZYNQ-7000 (ZC702, ZedBoard), STM32 Blue Pill, Raspberry Pi 4B

PROJECTS

AI-Driven EDA Tool for RTL Analysis & Verification

Tech : *Python, Verilog, SystemVerilog, ModelSim, TCL, LLMs*

Independent Research Project

Jan 2026 – Present

- Developing an AI-powered EDA tool leveraging LLMs for automated Verilog analysis, including syntax and functional error detection, code correction, and top-module extraction using AI-assisted reasoning.
- Architecting an end-to-end RTL design workflow integrating ModelSim-based simulation, waveform generation, and circuit visualization to enhance verification efficiency and streamline debugging.

Hardware Acceleration of Machine Learning Inference on FPGA for Binary Image Classification

Tech : *Python, Verilog, SystemVerilog, ModelSim, Xilinx Vivado, ZYNQ-7000, Cadence Genus*

Amrita School of Engineering, Bengaluru

Aug 2024 – Jun 2025

- Architected a UVM-based verification environment for 3 RTL compute modules (CNN, k-NN, Decision Tree) comprising UVM agent, driver, monitor, scoreboard, and coverage collector; applied constrained-random stimulus via virtual interfaces and SVA assertion suites to achieve 96% functional and code coverage closure across all DUTs prior to FPGA deployment.
- Isolated and resolved 4 pre-synthesis RTL defects — including a critical data-alignment hazard in the CNN inference pipeline — using ModelSim/QuestaSim waveform debug and SVA assertion analysis; cross-validated DUT outputs against Python golden reference models to ensure cycle-accurate behavioral correctness.
- Performed RTL-to-netlist synthesis using Cadence Genus targeting Xilinx ZYNQ-7000; conducted post-synthesis gate-level simulation (GLS) on ZC702/ZedBoard and executed PPA analysis to evaluate area-power-timing trade-offs across CNN, k-NN, and Decision Tree accelerator architectures.

Evaluation of Convolutional Neural Network Architectures for Fruit Ripeness

Tech : *Python, ResNet50, EfficientNetB0, Image processing*

Amrita School of Engineering, Bengaluru

Aug 2024 – Dec 2024

- Evaluated EfficientNetB0 vs. ResNet50 for multi-class fruit ripeness classification; top model achieved 78.67% test accuracy, a 13.35% improvement over baseline on the same dataset. — **Published in IEEE Xplore.**

Design and Optimization of Low-Power Adder Architectures

Tech : CMOS Design, Verilog, Cadence Tools

Amrita School of Engineering, Bengaluru

Feb 2024 – May 2024

- Designed and synthesized mux-based ripple carry adder architectures in Verilog; benchmarked PPA metrics using Cadence Genus across multiple design variants, evaluating critical path delay and power-area trade-offs.
- Applied clock gating and operand isolation to reduce switching activity; achieved ~ 18% reduction in dynamic switching power over the baseline design while maintaining timing closure at the target frequency.

WORK EXPERIENCE

Jr. Embedded Systems Engineer

Jul 2025 – Present

7s Technologies, Hyderabad

- **Turnstile Control System (Raspberry Pi 4B)**
 - Developed embedded firmware for a QR-based turnstile control system on Raspberry Pi 4B; integrated real-time server authentication over TCP/IP with GPIO-controlled actuation logic, enabling timed 10-second gate release upon successful credential validation.
 - Implemented fault-handling routines for network timeouts and invalid QR payloads, ensuring fail-secure operation across all edge cases.
- **Multi-Drone Battery Management System (STM32 – Blue Pill)**
 - Designed and implemented an automated battery handling system for a multi-drone fleet using STM32 (Blue Pill); engineered an X-Y Cartesian positioning mechanism with stepper motor control for sub-millimeter slot alignment and mechanical stabilization.
 - Implemented actuator control logic for automated battery insertion and extraction and architected a multi-slot charging controller supporting up to 12 batteries simultaneously with coordinated power sequencing. Enabled reliable inter-device communication using RS-485/Modbus protocol for synchronized data exchange across the charging array.

EDUCATION

Amrita Vishwa Vidyapeetham

Master's Degree in VLSI Design CGPA: 7.53

Bengaluru, India

Aug 2023 – Aug 2025

Sagi Rama Krishnam Raju (SRKR) Engineering College

Bachelor's Degree in Electronics and Communication Engineering (ECE) CGPA: 6.77

Bhimavaram, India

Aug 2019 – Jun 2023

PUBLICATIONS

1. Accelerating Lightweight Binary Image Classification on FPGA Using Machine Learning Models.

<https://ieeexplore.ieee.org/document/11233695>

2. Ripeness Revolution: Harnessing CNN Models for Precise Fruit Classification.

<https://ieeexplore.ieee.org/document/11070765>

3. Determining the Fruit Ripening Stage Using Convolution Neural Networks.

<https://link.springer.com/chapter/10.1007/978-981-99-4577-113>

CERTIFICATIONS + ACHIEVEMENTS

VLSI Chip Design with CPS for Industrial Applications

Coursera

Mar 2025
coursera.org/share/4a24f13b3c5af5d90e60dce7ee4ae0385

Chip-based VLSI Design for Industrial Applications

Coursera

Jan 2025
coursera.org/share/76842361dda3e5fa4535a4ea0d3838f9

MSME Innovation Scheme 2022 — Government-Funded Rs. 8 Lakhs Grant

Secured competitive national funding for a drone-based disaster response system featuring real-time aerial monitoring, AI-driven image analysis, and autonomous search-and-rescue support; delivered centralized sensor fusion and decision-support workflows adopted for emergency response logistics. | [Project Approval Form](#)